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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
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10/714,386

11/14/2003

Andrew H. Barr

200308581-1

3950

22879 7590 08/06/2007

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EXAMINER

BHAT, ADITYA S

ART UNIT

PAPER NUMBER

2863

MAIL DATE

DELIVERY MODE

08/06/2007

PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No. 10/714,386	Applicant(s) BARR ET AL.	
	Examiner Aditya S. Bhat	Art Unit 2863	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 23 May 2007.
- 2a) ☐ This action is **FINAL**. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 1-20 is/are pending in the application.
- 4a) Of the above claim(s) _____ is/are withdrawn from consideration.
- 5) ☐ Claim(s) _____ is/are allowed.
- 6) ☒ Claim(s) 1-20 is/are rejected.
- 7) ☐ Claim(s) _____ is/are objected to.
- 8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☒ The drawing(s) filed on 14 November 2003 is/are: a) ☒ accepted or b) ☐ objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All b) ☐ Some * c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
 2. ☐ Certified copies of the priority documents have been received in Application No. _____.
 3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- | | |
|--|---|
| 1) <input checked="" type="checkbox"/> Notice of References Cited (PTO-892) | 4) <input type="checkbox"/> Interview Summary (PTO-413)
Paper No(s)/Mail Date. _____ |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948) | 5) <input type="checkbox"/> Notice of Informal Patent Application |
| 3) <input type="checkbox"/> Information Disclosure Statement(s) (PTO/SB/08)
Paper No(s)/Mail Date _____ | 6) <input type="checkbox"/> Other: _____ |

DETAILED ACTION

Allowable Subject Matter

The indicated allowability of claims 1-8 & 15-20 is withdrawn in view of the newly discovered reference(s) Adamane et al. (USPN 2003/0115385). Rejections based on the newly cited reference(s) follow.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

Claims 1-20 are rejected under 35 U.S.C. 103(a) as being unpatentable over Adamane et al. (USPN 2003/0115385).

With regards to claim 1, Adamane et al. (USPN 2003/0115385) teaches a computer system comprising: a processor(101) configured to execute an operating system;(Page 2, paragraph 0022)

a memory controller coupled to the processor;(101;fig 1)

a memory coupled to the memory controller;(101,104,108;fig 1)

a first input/output (I/O) controller coupled to the memory controller;(101,118 fig1)

a first expansion slot coupled to the first I/O controller;(101,118;fig 1) and

a test module directly coupled to the first expansion slot; (Page 1, paragraph 0005)

wherein the test module is configured to obtain access to a portion of the memory from the operating system, and wherein the test module is configured to cause tests to be

performed on the portion of the memory using direct memory access (DMA) subsequent to obtaining access to the portion of the memory. (Page 1, paragraph 0015)

With regards to claim 2, Adamane et al. (USPN 2003/0115385) teaches the processor is configured to cause the operating system to be booted, and wherein the test module card is configured to cause the tests to be performed on the portion of the memory subsequent to the operating system being booted. (Page 1, paragraph 0011 & 0015)

With regards to claim 3, Adamane et al. (USPN 2003/0115385) teaches the test module card is configured to cause the tests to be performed on the portion of the memory during execution of the operating system. (Page 1, paragraph 0011 & 0015)

With regards to claim 4, Adamane et al. (USPN 2003/0115385) teaches a second I/O controller coupled to the memory controller; a second expansion slot coupled to the second I/O controller; and an I/O device coupled to the second expansion slot. (fig 1)

With regards to claim 5, Adamane et al. (USPN 2003/0115385) teaches the test module card is configured to cause tests to be performed on the memory by providing read and write transactions to the first I/O controller. (Page 2, paragraph 0023)

With regards to claim 6, Adamane et al. (USPN 2003/0115385) teaches the read and write transactions comprise DMA transactions. (Page 1, paragraph 0023)

With regards to claim 7, Adamane et al. (USPN 2003/0115385) teaches a bus bridge coupled to the processor and the first I/O controller. (114; fig 1)

With regards to claim 8, Adamane et al. (USPN 2003/0115385) teaches a system controller that comprises the memory controller. (101;fig 1)

With regards to claim 9, Adamane et al. (USPN 2003/0115385) teaches obtaining access to a portion of a memory of a computer system from an operating system during operation of a computer system; (Page 1, paragraph 0015)
generating a test transaction in a test module directly coupled to an expansion slot of the computer system; (Page 1, paragraph 0004 & 0015) and
providing the test transaction to the portion using direct memory access (DMA) to cause information to be read from or stored into the portion subsequent to obtaining access to the portion of the memory. (Page 1, paragraph 0015)

With regards to claim 10, Adamane et al. (USPN 2003/0115385) teaches detecting an error that occurs in response to the test transaction; and performing a remedial action associated with the portion in response to detecting the error. (Page 1, paragraph 0015)

With regards to claim 11, Adamane et al. (USPN 2003/0115385) teaches providing the test transaction from the test module to an I/O controller coupled to the expansion slot; (118 fig 1)
providing the test transaction from the I/O controller to a bus bridge;(114 fig 1)
providing the test transaction from the bus bridge to a system bus; (112 fig 1)
providing the test transaction from the system bus to a memory controller; (101 fig 1)and
providing the test transaction from the memory controller to the portion. (104,106; fig 1)

With regards to claim 12, Adamane et al. (USPN 2003/0115385) teaches storing information in the memory in response to the test transaction being a write transaction. (Page 2, paragraph 0021)

With regards to claim 13, Adamane et al. (USPN 2003/0115385) teaches in response to the test transaction being a read transaction:

providing information associated with the test transaction from the portion to the memory controller; (Page 1, paragraph 0015) providing the information from the memory controller to the system bus; providing the information from the system bus to the bus bridge; providing the information from the bus bridge to the I/O controller; and providing the information from the I/O controller to the test module. (see fig 1)

With regards to claim 14, Adamane et al. (USPN 2003/0115385) teaches providing the test transaction from the test module to an I/O controller coupled to the expansion slot; providing the test transaction from the I/O controller to a system controller; providing the test transaction from the system controller to a memory controller; and providing the test transaction from the memory controller to the portion. (fig 1)

With regards to claim 15, Adamane et al. (USPN 2003/0115385) teaches computer system comprising:

a processor; (101 fig 1)

a memory controller coupled to the processor and configured to perform error correction; (101 fig 1)

a memory coupled to the memory controller; (fig 1)

an input/output (I/O) controller coupled to the memory controller;(101,118; fig 1)
an expansion slot coupled to the I/O controller; 118 and
a card directly coupled to the expansion slot; (Page 1, paragraph 0004)
wherein the test module card is configured to obtain access to a portion of the
memory from an operating system, and wherein the test module card is configured to
cause tests to be performed on the portion of the memory by providing read
transactions associated with the memory to the I/O controller subsequent to obtaining
access to the portion of the memory. (Page 1, paragraph 0015)

With regards to claim 16, Adamane et al. (USPN 2003/0115385) teaches the
operating system;
wherein the processor is configured to cause the operating system to be booted, and
wherein the test module is configured to cause the tests to be performed on the memory
using DMA subsequent to the operating system being booted. (Page 1, paragraph 0011
& 0015)

With regards to claim 17, Adamane et al. (USPN 2003/0115385) teaches the
operating system;
wherein the processor is configured to cause the operating system to be executed, and
wherein the test module is configured to cause the tests to be performed on the memory
using DMA during execution of the operating system. (Page 1, paragraph 0011 & 0015)

With regards to claim 18, Adamane et al. (USPN 2003/0115385) teaches the I/O
controller provides the read transactions to a system bus. (fig 1)

With regards to claim 19, Adamane et al. (USPN 2003/0115385) teaches the test module card is configured to cause tests to be performed on the memory using direct memory access (DMA). (Page 1, paragraph 0015)

With regards to claim 20, Adamane et al. (USPN 2003/0115385) teaches the read transactions comprise direct memory access (DMA) transactions. (Page 1, paragraph 0015)

Adamane et al does not appear to explicitly teach a test module card.

Adamane et al does teach I/O cards (Page 1, paragraph 0004) and testing a I/O device. (Page 1, paragraph 005)

It would've been obvious to one skilled in the art at the time of the invention to use a test module card to test the I/O device in order to determine that it is functioning normally.

Response to Arguments

Applicant's arguments with respect to claim 1-20 have been considered but are moot in view of the new ground(s) of rejection.

Conclusion

The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. Poisner (USPN 5,890,012) teaches a system for programming peripheral with address and direction information and sending the information through data bus or control line when DMA controller asserts data knowledge line and Kulkarni (USPN 5,551,006) teaches low cost write through cache coherency apparatus and method for computer systems without a cache supporting bus.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Aditya S. Bhat whose telephone number is 571-272-2270. The examiner can normally be reached on M-F 9-5:30.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, John Barlow can be reached on 571-272-2269. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.



Aditya Bhat
July 30, 2007